1703 E. Highway 50 Yankton, SD 57078 USA
Phone: 800-762-8800 or 605-665-9321 Fax: 605-665-1709
Website: www.mtronpti.com

SPECIFICATION FOR 2.5 x 2.0 mm HCMOS COMPATIBLE SMT OSCILLATOR
MtronPTI P/N M2502S004

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O		100.000000		MHz	
Frequency Stability						
Frequency Stability	ΔF/F	-50		+50	ppm	Includes calibration at +25C plus deviation vs. temperature.
RF Output						
Output Type		HCMOS Compatible				
Output Load				15	pF	
Symmetry (duty cycle)	T_{DC}	45		55	%	Ref to ½ V_{DD}
Logic "1" Level	V_{OH}	90% V_{DD}			V	HCMOS load
Logic "0" Level	V_{OL}			10% V_{DD}	V	HCMOS load
Rise/Fall Time	T_R/T_F			5	ns	From 10% to 90% V_{DD}
Start-Up Time				10	ms	
Standby Logic "1"		70% V_{DD} or N/C			V	Pad 1: Output Enabled
Standby Logic "0"				30% V_{DD}	V	Pad 1: Output Disabled to high impedance
Supply Voltage & Power Consumption						
Operating Voltage	V_{DD}	1.62	1.80	1.98	V	
Operating Current	I_{DD}			16	mA	

Environmental & Mechanical Requirements:

Operating Temperature	T_A	-40		+85	°C	
Storage Temperature	T_S	-55		+125	°C	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Cycle	Per MIL-STD-883, Method 1010, B (-55°C to 125°C, 15 min. dwell, 10 cycles)					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1					
Package Type	2.0 X 2.5 X 1.0 mm, 4-pad leadless ceramic. RoHS 6/6 compliant					

1703 E. Highway 50 Yankton, SD 57078 USA
Phone: 800-762-8800 or 605-665-9321 Fax: 605-665-1709
Website: www.mtronpti.com

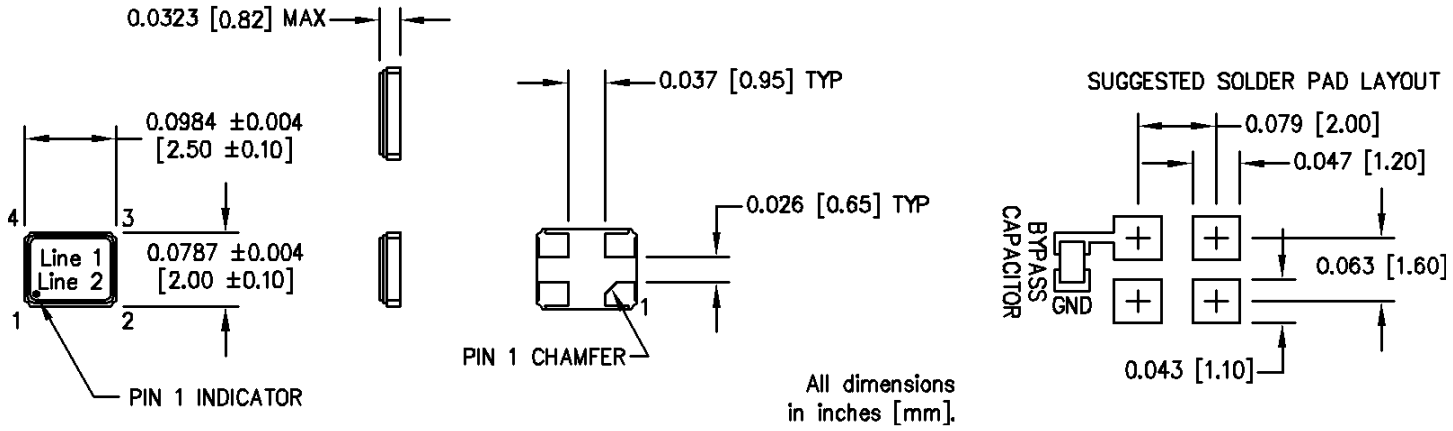
SPECIFICATION FOR 2.5 x 2.0 mm HCMOS COMPATIBLE SMT OSCILLATOR
MtronPTI P/N M2502S004

Dimensions, Marking, and Pin Out Information:

Pad	Function
1	Standby
2	Ground
3	Output
4	$+V_{DD}$

Part Marking	
Line 1	100M000
Line 2	M ywwv

Legend	
y	Year
ww	Work week
V	Factory code



Note : Layout should include 0.01 µF or larger bypass capacitor between +Vdd and ground.

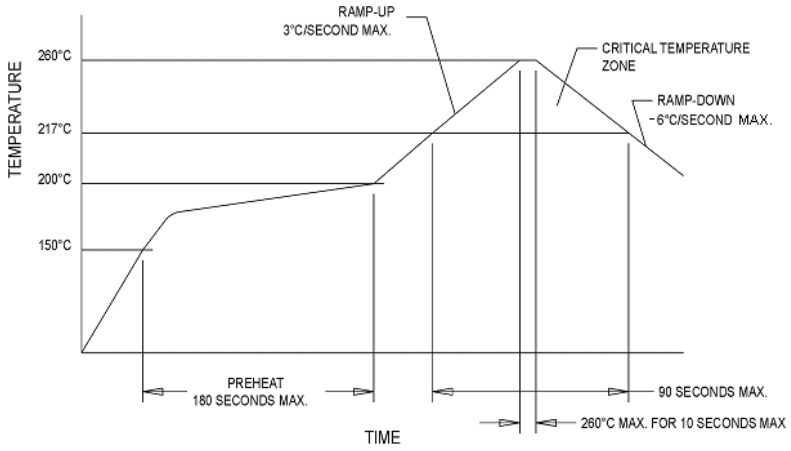


Figure 1

Datasheet Revision Table:

Date	Rev.	Author	Details of Revision
07-24-19	A	BRR	Preliminary Release