



SPECIFICATION FOR LVPECL VCXO MtronPTI P/N: M3028S003

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F _o		156.250000		MHz	
Frequency Stability						
Frequency Stability		-50		+50	ppm	Includes initial tolerance with V _c = 1.65, deviation over temperature, voltage, and aging
Aging		-3		+3	ppm	first year
		-10		+10		Over 15 years includes 1 st year.
RF Output						
Output Type		PECL				
Output Load		50 ohms to (V _{cc} -2)V or Thevenin equivalent				
Symmetry (duty cycle)	T _{DC}	45		55	%	@ 50% of waveform
Logic Level "1"		V _{cc} -1.08			V	
Logic Level "0"				V _{cc} -1.63	V	
Rise/Fall Time	T _R /T _F			0.35	ns	From 20% to 80% of waveform
Output Enable Logic		70% V _{cc} or N/C			V	Pad 2. Output enabled
Output Disable Logic				30% V _{cc}	V	Pad 2. Output to high-Z
Startup Time			3	10	ms	
Frequency Adjustment						
Absolute Pull Range (APR)		±80			ppm	Referenced to nominal frequency, including deviation over temperature, aging, shock, vibration, supply voltage
Control Voltage		0.00	1.65	3.30	V	Pad 1
Tuning Slope			90		ppm/V	
Linearity				10	%	
Modulation Bandwidth	f _m	10			kHz	-3 dB
Input Impedance	Z _{IN}	500			kΩ	Pad 1
Supply Voltage & Power Consumption						
Operating Voltage	V _{CC}	3.13	3.30	3.47	V	
Operating Current	I _{CC}			75	mA	
Other Parameters						
Phase Jitter	Φ _J			0.40	ps	integrated phase noise, 12 kHz – 20 MHz

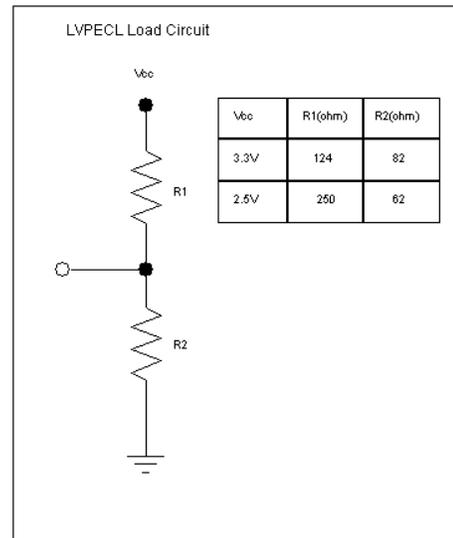
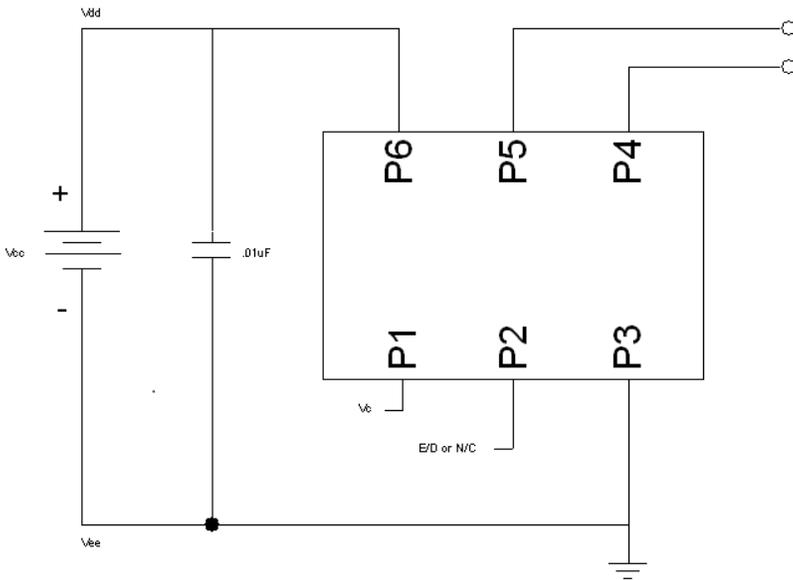


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Environmental & Packaging Requirements:

Operating Temperature	T _A	-40		+85	°C	
Storage Temperature	T _S	-55		+125	°C	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Cycle	Per MIL-STD-883, Method 1010, B (-55°C to 125°C, 15 min. dwell, 10 cycles)					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁸ atm cc/s of Helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1.					
Package Type	5 X 7 mm 6-pad leadless ceramic. RoHS compliant.					

Typical LVPECL Test Circuit & Load Circuit Diagrams:





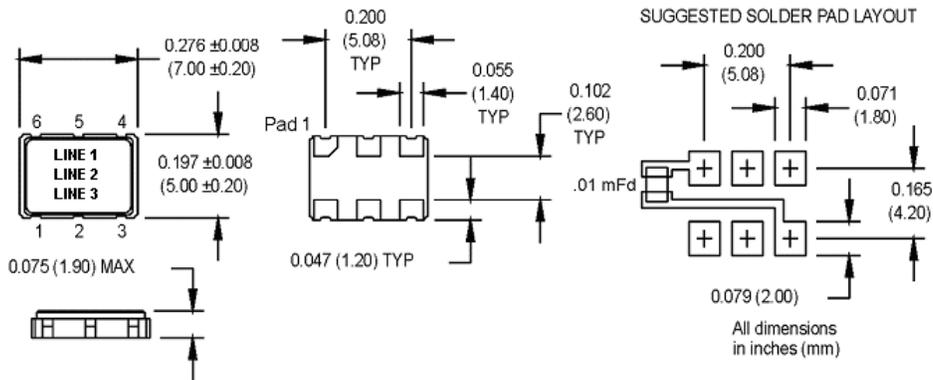
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Marking, Pin Out & Dimensions:

Pad	Function
1	Control Voltage
2	Tristate Control
3	Ground
4	Output 1
5	Output 2
6	+V _{CC}

Part Marking	
Line 1	M3028S003
Line 2	156M2500
Line 3	M yy ww vv

Legend	
yy	Year
ww	Work week
vv	Factory code



Soldering Conditions:

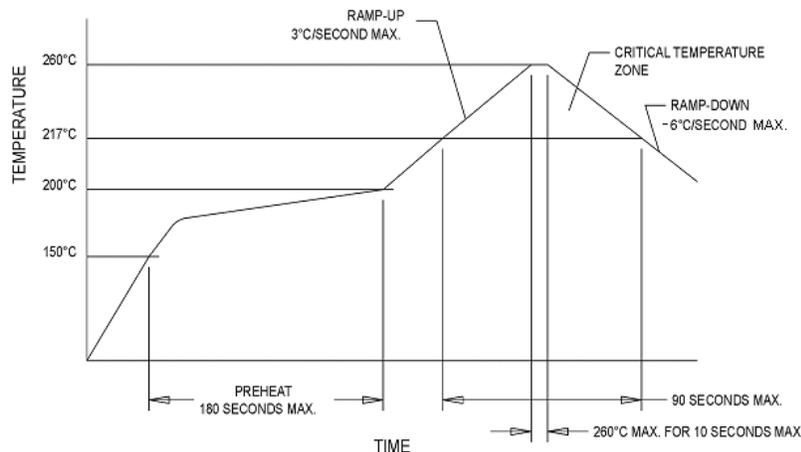


Figure 2

DATA SHEET REVISION TABLE:

Date	Rev.	Author	Details of Revision
10/14/15	0	DCO	Original release