MtronPTI
...when timing matters

SPECIFICATION FOR LVPECL VCXO
MtronPTI P/N: M3028S004

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O		122.880000		MHz	
Frequency Stability						
Frequency Stability		-25		+25	ppm	Includes initial tolerance with Vc = 1.65, deviation over temperature, voltage
Aging		-5		+5	ppm	first year
		-3		+3		per year after first year
RF Output						
Output Type		PECL				
Output Load		50 ohms to (Vcc-2)V or Thevenin equivalent				
Symmetry (duty cycle)	T_{DC}	45		55	%	@ 50% of waveform
Logic Level "0"				Vcc-1.63	V	
Logic Level "1"		Vcc-1.085			V	
Rise/Fall Time	T_R/T_F		0.3	1.0	ns	From 20% to 80% of waveform
Startup Time				10	ms	
Tristate Function		70% Vcc or N/C				Pad 2: Clock signal outputs
				30% Vcc		Pad 2: Output disable to High-Z
Frequency Adjustment						
Absolute Pull Range (APR)		±40			ppm	Referenced to nominal frequency, including deviation over temperature, aging, shock, vibration, supply voltage
Control Voltage		0.00	1.65	3.30	V	Pad 1
Linearity				10	%	
Modulation Bandwidth	fm	10	20		kHz	-3 dB
Input Impedance	Z_{IN}	100			kΩ	Pad 1
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.13	3.30	3.47	V	
Operating Current	I_{CC}			80	mA	
Other Parameters						
Phase Noise			-128		dBc/Hz	@ 1 kHz
			-150			@ 10 kHz
			-157			@ 100 kHz
			-157			@ 1 MHz
Phase Jitter	ΦJ		0.1		ps	12 kHz – 20 MHz

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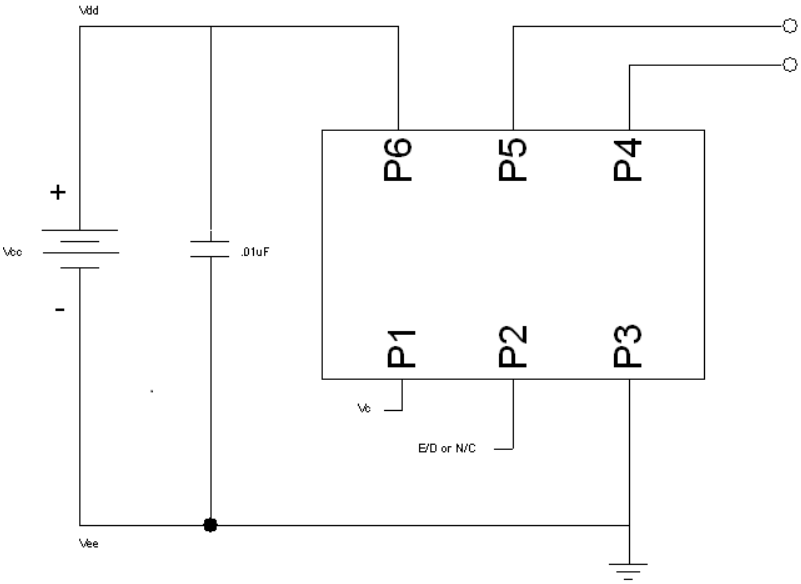
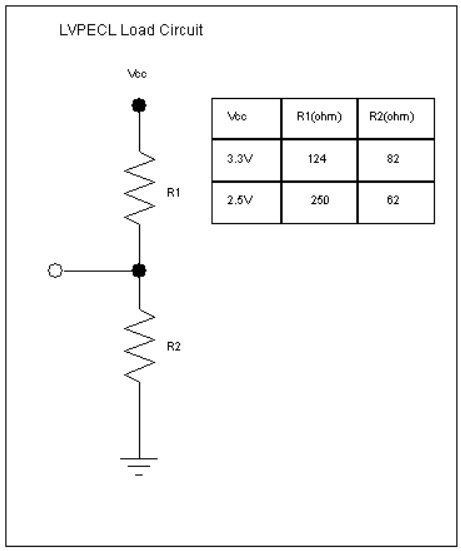
Environmental & Packaging Requirements:

Operating Temperature	T_A	-40		+85	°C	
Storage Temperature	TS	-55		+125	°C	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Cycle	Per MIL-STD-883, Method 1010, B (-55°C to 125°C, 15 min. dwell, 10 cycles)					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1.					
Package Type	5 X 7 mm 6-pad leadless ceramic. RoHS compliant.					

Typical LVPECL Test Circuit & Load Circuit Diagrams:





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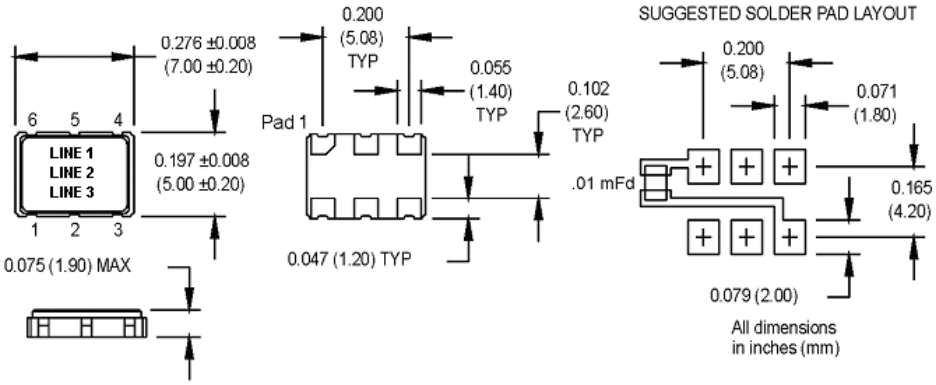
Marking, Pin Out & Dimensions:

Pad	Function
1	Control Voltage
2	Tristate Control
3	Ground
4	Output 1
5	Output 2
6	+V_{CC}

Part Marking	
Line 1	M3028S004
Line 2	122M8800
Line 3	M yy ww vv

Legend	
yy	Year
ww	Work week
vv	Factory code



Soldering Conditions:

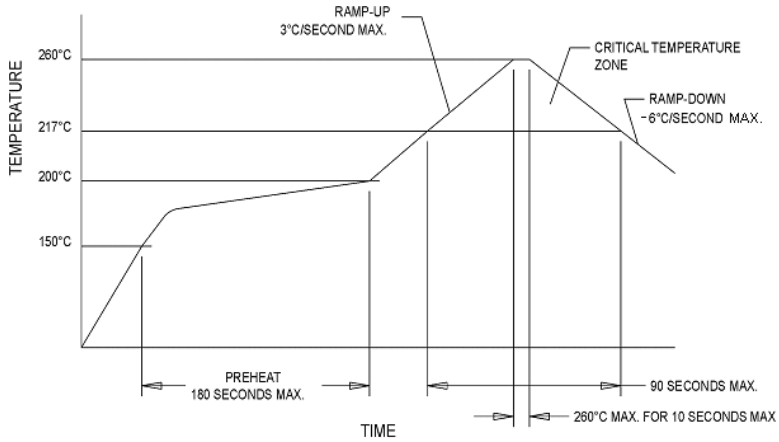


Figure 2

DATA SHEET REVISION TABLE:

Date	Rev.	Author	Details of Revision
04/21/16	0	MM	Original release
04/08/16	A	MM	Error corrections.